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Carrier-Based Digital PWM and Multirate Technique of a Cascaded H-Bridge Converter for Power Electronic Traction Transformers

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***Abstract*—In the existing technique for power electronic converters with low switching frequency and multiple cells, the sampling frequency is always set at the same value as the control frequency, and the modulating wave in each cell updates itself when its corresponding carrier reaches its peak and valley. In this paper, this implementation scheme is denoted as AS-PWM. It is proved that AS-PWM suffers from three defects: further increase of switching frequency is restricted by the available control period and the total cell number; long modulator delay exists and may bring the control system into instability if high cross-over frequency is chosen; and spectrum aliasing towards digital modulating waves may occur and makes the ac input current distorted. Therefore, another implementation scheme of carrier-based digital PWM (DPWM) is recommended in this paper, which is denoted as MS-PWM. In MS-PWM, all of the modulating waves update themselves at the same time. The research presented in this paper is based on a power electronic traction transformer (PETT), which is made up of a cascaded H-bridge (CHB) converter and several DC/DC converters. For the consideration of scalability, control and reliability, a star-connected distributed control system is adopted for the PETT equipment. In order to make full use of this distributed hardware, and to improve the control performance with relatively low requirement towards the digital chips, a universal-type multirate structure is proposed in this paper, which is based on the MS-PWM technique. In the proposed structure, the sampling frequency, control frequency and modulating-wave updating frequency can be separated from the switching frequency, and each of them can be chosen independently according to the practical control demand and the hardware condition. There is no mutual effect between their selections. The influence of the variation of these three frequencies on the control performance is analyzed as well. At last, experiment results based on a five-cell PETT laboratory prototype with rated power of 30 kW are provided, and all of them verify the effectiveness and correctness of the proposed algorithms.**

***Index Terms*—Digital PWM, aliasing, stability, multirate, power electronic traction transformer.**

NOMENCLATURE

N	Total cell number of CHB.
v_g	AC input voltage.
i_g	AC input current.
v_{convj}	PWM voltage of Cell j, where $j = 1, 2, \cdots, N$.
v_{dcj}	DC output voltage of Cell j..
v_{ctr} (v_{ctr}^{j})	Analog modulating wave (of Cell j).
v_{ctr}^{d} (v_{ctr}^{dj})	Digital modulating wave (of Cell j).
v_{ctr}^{b} (v_{ctr}^{bj})	Quantized boxcar modulating wave (of Cell j).
f_{sw}	Switching frequency.
f_{ctr}	Control frequency.
f_{sa}	Sampling frequency.
$f_{sa,dc}$	Sampling frequency of v_{dcj}.
$f_{sa,ac}$	Sampling frequency of v_g ($f_{sa,ac}^{2}$) and i_g ($f_{sa,ac}^{1}$)
f_{ud}	Modulating-wave updating frequency.
f_{ud}^{1}	f_{ud} in the universal-type structure.
f_{ud}^{2}	f_{ud} in the simplified structure.
f_{trm}	Data transmission frequency.
$f_{lw,max}$	Maximum frequency of low-frequency components of v_{ctr}^{d}.
T_{sw}	Switching period, $1/f_{sw}$.
T_{ctr}	Effective control period, $1/f_{ctr}$.
$T_{d,ca}$	Computation delay.
$T_{d,net}$	Transmission delay.
M	Down-sampling coefficient.
L	Up-sampling coefficient.
$G_h^a(s)$	ZOH model of AS-PWM.
$G_h^b(s)$	ZOH model of MS-PWM.
$DecFlt(z)$	Decimation filter.
$ItpFlt(z)$	Interpolation filter.
AS-PWM	Asymmetrically-sampled PWM.
MS-PWM	Multi-sampled PWM.

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I. INTRODUCTION

POWER electronic traction transformer (PETT) is the core component of next generation high-speed trains, which can replace the line-frequency traction transformer and four-quadrant traction converter now available on board. Through the high-frequency conversion technique, PETT can substantially reduce the axle loads, the installation space and the energy consumption [1]-[3]. In order to improve the scalability, control performance and long-term reliability of the PETT, it is significant to develop an optimal digital control structure. In general, there are two available structures of digital control system: centralized control structure and distributed control structure. A single controller is adopted in the centralized control structure, where sampling, calculation and PWM are all executed in the same controller [4]. Although the centralized control structure is quite simple, it leads to poor

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scalability, and meanwhile, a large quantity of sampling connection lines and optical fibers makes the layout quite chaotic. What's more, it is unqualified for more complicated control task and communication requirement (communicate with the upper system, for example, the traction control unit on board). In order to overcome the above shortcoming, double-layers control structure including a main controller and several slave controllers is adopted in the distributed control system. There are three different kinds of distributed control structure: star-connected, bus-based and ring-type [5]. The later two are more suitable for the MMC-based (Modular Multilevel Converter) HVDC system. The number of cascaded cells in a certain HVDC system is always much larger than that in PETT. By use of bus-based or ring-type structure, a large number of communication lines between the main controller and slave controllers can be avoided [6]. However, as the cell number of a PETT is much less than that of a HVDC system, the above advantage is hard to be highlighted. Therefore, in this paper, the star-connected distributed control structure is adopted for the PETT. In Section II, the basic structure of the digital control system for a PETT are introduced briefly.

The PETT is made up of a cascaded H-bridge (CHB) converter and several output-parallel DC/DC converters [2], [7]-[8], [35]. As the rated power of the PETT is generally high in practice, the switching frequency of the CHB is always low [2]. In order to improve the control performance of a low-switching-frequency converter, it can adopt the model predictive control approach [9]-[11], or reduce the modulator delay [9], [12]-[17]. For the later one, the earliest publication can be found in [12]-[13], where a multi-sampled PWM (MS-PWM) is proposed. In MS-PWM, the modulating-wave updating frequency can be higher than the switching frequency. However, as the modulating wave in the PWM is ladder-shaped, extra pulses or multi-switching cannot be avoided in the MS-PWM. In order to settle this problem, another kind of modulating-wave updating scheme is proposed in [18], in which the modulating wave in each cell updates itself when its corresponding carrier reaches its peak and valley. For the sake of analysis, according to [19], this scheme is named as asymmetrically-sampled PWM (AS-PWM). Recently, the limitation of AS-PWM is reported in [20]-[21], [36]. It is indicated that the low-order harmonics may be brought into the PWM voltage by applying AS-PWM. However, as the discovery in the above publications is presented qualitatively, the limitation towards AS-PWM is analyzed again in this paper. With quantitative analyses, it is proved that there are three defects in AS-PWM:

1) There is a strong correlation between the switching frequency and the available control period or/and the total cell number. For instance, if there are more cells, it may have to select a lower value of the switching frequency;

2) There is a long modulator delay. It will worsen the control performance and the system stability. Especially when a high value of gain cross-over frequency is chosen, the system may be unstable;

3) The spectrum aliasing towards the *digital modulating waves* may occurs. It will result in the distortion of ac input current.

These three defects may restrict the application of AS-PWM in the low-switching-frequency and multi-cell system. To our knowledge, in practice, there are still three methods to address these defects. The first method is to select suitable value of control frequency and modulating-wave updating frequency to avoid the down-sampling effect, which won't increase the modulator delay but can suppress the spectrum aliasing. The second method is to reduce the bandwidth of feedback-control-loop to make the system stable by adjusting control parameters. The third method is to select a suitable value of switching frequency, which is higher than the dominating frequency of harmonics, to suppress the spectrum aliasing. However, these methods still suffer other bad effect. For the first method, it brings the mutual effect between the control and the selecting of switching frequency, which sometimes is quite inconvenient. For the second method, the dynamic response may be seriously deteriorated. For the third method, it has to choose a relatively high value of switching frequency.

On the contrary, MS-PWM is immune to all above three defects, therefore, it is recommended in this paper. Detailed analysis and description are presented in Section III. As for the problem of extra pulses, the basic idea to eliminate them is briefly introduced in Appendix. Through the field programmable gate array (FPGA) [14], the extra pulses can be eliminated conveniently.

However, even MS-PWM is adopted, the further development of the control performance is still restricted by the available control period, or more essentially the available digital chips. This problem is especially prominent in the PETT system. As the PETT is a two-stage multi-cell converter, a lot of control tasks need to be executed. What's more, in order to improve the reliability of the PETT equipment, condition monitoring, fault diagnosis and fault tolerance are urgent and imperative [22]-[24]. In this case, if all of the algorithms are carried out in the same digital chip, relatively long control period or relatively low control frequency cannot be avoided. In other word, there is contradiction between the improvement of control performance and the finite time-resource occupation of digital chips.

Considering that there are several digital chips in the PETT control system, and the sampling, control and modulation are relatively independent with each other, a universal-type multirate structure is proposed in Section IV. In this structure, the sampling, the execution of the main control algorithms, and the modulation can be processed in different digital control chips, and the frequencies of these three links can be different with each other. The selection principles of these three frequencies are introduced in Section IV. There are several advantages to separate the sampling, control and modulation links:

1) It can reduce the resource occupation of digital chip which is responsible for the execution of main control algorithms;

2) If the control frequency is relatively low, it can select relatively high sampling frequency and modulating-wave updating frequency with the same low control frequency to improve the steady-state control performance;

3) In this case, the distributed hardware can better match the distributed software, and then high efficient utilization of digital chips and good control performance of the PETT can be achieved at the same time.

As the dominant frequencies of the sampling, control and modulation are different with each other, the up-sampler, down-

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sampler and frequency conversion filter are needed between these three links. The principle of down-sampler and up-sampling are respectively presented in Section III and Section IV. The first contribution of this paper is to compare AS-PWM and MS-PWM and to reveal the defects of AS-PWM. The second contribution is to develop a universal-type multirate technique suitable for PETT system, which can compromise the contradiction between control performance and available digital chips.

Based on a five-cell PETT laboratory prototype with rated power of 30 kW, the experiment results are given in Section V. Finally, the conclusion of this paper is provided in Section VI.

II. Digital Control System of a PETT

The topology of a PETT is shown in Fig. 1. The PETT is a complicated system, which is made up of a CHB converter in the front end and several DC/DC converters in the backward stage. There are N cells in the PETT.

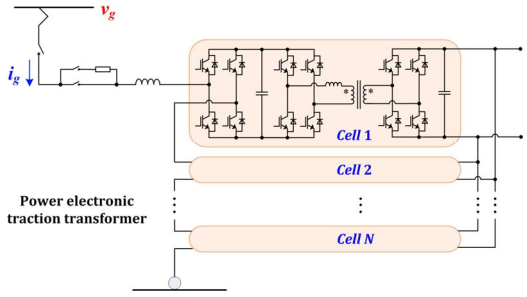

Fig. 1. The topology of a PETT.

In order to improve the scalability, control performance and long-term reliability of the PETT equipment, a two-layer control structure is adopted, including the converter-layer controller (or main controller) and the cell-layer controllers (or slave controllers), as shown in Fig. 2. The slave controllers are responsible for sampling the cell-layer voltages and currents, processing the PWM of the CHB in each cell and the phase-shift modulation (or frequency modulation) of DC/DC converters, and executing the cell-layer fault-diagnosis and protection. The main controller is responsible for controlling the PETT and communicating with the upper system like traction control unit [25]. The control tasks for a PETT includes sampling of converter-layer voltages and currents, phase locking and synchronization, regulating the dc voltages and the ac input current of the CHB, regulating the output dc voltage of DC/DC converters, processing the power balance control of the PETT [26], and executing the converter-layer fault-diagnosis and protection [22]-[24]. The communication between the main controller and each slave controller is through the optical fibers, and there is no communication interconnection between different slave controllers. At a certain interval, each slave controller sends its sampling values to the main controller, and the main controller sends its calculation results back to the slave controllers. The main controller is made up of two digital signal processors (DSPs) and a FPGA (which are noted as *m*DSP1, *m*DSP2 and *m*FPGA respectively), while each slave controller is made up of a DSP and a FPGA (which are noted as *s*DSP-*j* and *s*FPGA-*j* respectively, where j =1, 2, …). In the main controller, *m*DSP2 is used for controlling the PETT, while *m*DSP1 is used for communicating with the upper control system. In this paper, the control frequency is denoted as f_{ctr}, and the data transmission frequency is denoted as f_{trm}. In order to avoid the conflict of interrupts and the crowd with channels, the control frequency of the CHB is selected the same value as the control frequency of DC/DC converters, and the data transmission frequency is the same as the control frequency, that is $f_{ctr} = f_{trm}$.

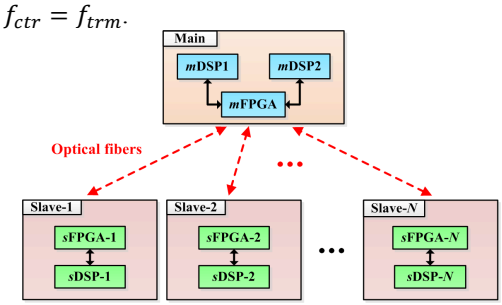

Fig. 2. The basic structure of the digital control system for the PETT.

III. Implementation Schemes of Carrier-Based DPWM

For the sake of analysis, in the following paper, a two-cell CHB converter is taken as an instance to investigate the influence of different implementation schemes of carrier-based DPWM on the control performance and the system stability. The circuit diagram of a two-cell CHB converter is shown in Fig. 3. L_g is the ac input filter inductor, C_{gj} is the dc output capacitor of Cell j; v_g is the ac input voltage, i_g is the ac input current (or the line current), v_{convj} is the PWM voltage of Cell j, v_{conv} is the total PWM voltage ($v_{conv} = v_{conv1} + v_{conv2}$), v_{dcj} is the dc output voltage of Cell j, $j = 1, 2$. As the traction supply network is always a weak gird, it is denoted as an ideal voltage source v_s and an inductor L_s in series.

Define the modulating wave of Cell j as v_{ctr}^j ($-1 < v_{ctr}^j < 1$), then $v_{convj} = v_{dcj} \times v_{ctr}^j$. Phase-shifted PWM (PS-PWM) technique is adopted to improve the equivalent switching frequency of ac input current i_g [27].

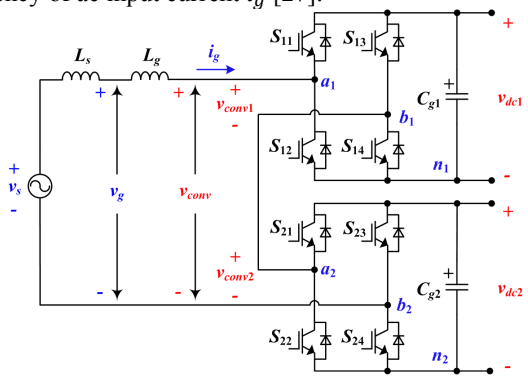

Fig. 3. The circuit diagram of a two-cell CHB converter.

A. Analog Modulating Wave, Discrete Modulating Wave, Digital Modulating Wave and Quantized Boxcar Modulating Wave

For the sake of analysis in the next part, it is necessary to introduce several concepts at first, including their physical meaning and the relationship between them. As shown in Fig. 4, the *discrete modulating wave* is generated by sampling the *analog modulating wave*, the *digital modulating wave* is generated by quantizing the *discrete modulating wave*, and the

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quantized boxcar modulating wave is generated from the *digital modulating wave* through a zero-order hold. That is to say, the *analog modulating wave* is a signal with continuous-amplitude and continuous-time characteristic; the *discrete modulating wave* is a signal with continuous-amplitude and discrete-time characteristic; the *digital modulating wave* is a signal with discrete-amplitude and discrete-time characteristic; and the *quantized boxcar modulating wave* is a signal with discrete-amplitude and continuous-time characteristic [28].

Therefore, the zero-order-hold (ZOH) effect of the DPWM is irrelevant to the modulation process, which just represents the relationship between the *digital modulating wave* and the *quantized boxcar modulating wave*. The small-signal model of the DPWM is certain and can be quantified. In some publication such as [9], [29], the ZOH model can be transformed as a pure delay model, and hence, is called as the modulator delay.

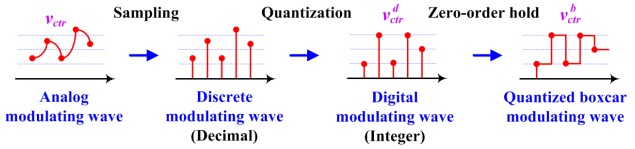

Fig. 4. The relationship of analog modulating wave, discrete modulating wave, digital modulating wave and quantized boxcar modulating wave.

B. Different Implementation Schemes of Carrier-Based DPWM

In order to reduce the modulator delay and improve the bandwidth of the control system, MS-PWM is proposed in [12]-[13]. In MS-PWM, the modulating-wave updating frequency f_{ud} is higher than the switching frequency f_{sw}. However, extra pulses may generate if MS-PWM is adopted [13]. The similar phenomenon is reported in [18], which is named as multi-switching. In order to avoid generating extra pulses, another implementation scheme of DPWM is proposed in [18]. For the sake of denoting, in this paper, the implementation scheme proposed in [18] is named as AS-PWM. Taking the two-cell CHB shown in Fig. 3 as an instance, the basic principle of AS-PWM is shown in Fig. 5(a), while the basic principle of MS-PWM is shown in Fig. 5(b).

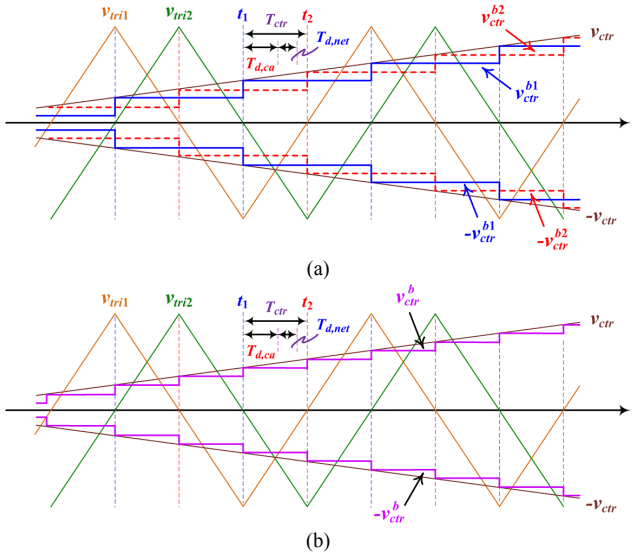

Fig. 5. Taking the two-cell CHB as an instance, different implementation schemes of carrier-based DPWM: (a) AS-PWM; (b) MS-PWM.

In Fig. 5(a), v_{tri1} is the carrier of Cell 1 while v_{tri2} is the carrier of Cell 2; v_{ctr} is the *analog modulating wave*; v_{ctr}^{b1} is the *quantized boxcar modulating wave* of Cell 1 while v_{ctr}^{b2} is the *quantized boxcar modulating wave* of Cell 2. v_{ctr}^{b1} and v_{ctr}^{b2} change themselves twice in every PWM carrier wave period (or switching period). It should be noticed that in the digital control system, the *analog modulating wave* v_{ctr} doesn't exist actually. Here, just for the convenience to analyze and explain, the *analog modulating wave* is constructed. In AS-PWM, v_{ctr}^{bj} $(j = 1, 2)$ updates itself when its corresponding carrier wave v_{trij} reaches its peak or valley. Therefore, from the point of each cell, the modulating-wave updating frequency of AS-PWM is $2f_{sw}$.

In Fig. 5(b), the *quantized boxcar modulating waves* of all of the cells are the same, which are all denoted as v_{ctr}^{b}. In MS-PWM, the updating time of v_{ctr}^{b} is irrelevant to the carrier wave v_{trij}, that is, the modulating-wave updating frequency is irrelevant to the switching frequency f_{sw}.

AS-PWM and MS-PWM will be compared below. It will be shown that there are three problems suffered by AS-PWM:

1) Upper Limitation of the Switching Frequency

As shown in Fig. 5(a), the effective control period of a two-cell CHB is $T_{ctr} = T_{sw}/4$, where T_{sw} is the PWM carrier wave period (or switching period). It can be inferred that for a N-cell CHB, the effective control period will be shortened as $T_{ctr} = T_{sw}/(2N)$. In the digital control system, the arithmetical and logical operation cannot be instantaneously executed but spend time, which is denoted as $T_{d,ca}$. For example, in Fig. 5(a), the voltages and currents are sampled in t_1; then after a certain time $(T_{d,ca} + T_{d,net})$, the control algorithms are executed and the new value of v_{ctr}^{b2} is generated and transmitted to the slave controller; and finally in t_2, the new value of v_{ctr}^{b2} is updated.

As shown in Section II, the two-layer control structure is adopted by the PETT, including the main controller and several slave controllers. In every switching period, the control algorithms are executed $2N$ times in the main controller, and then the calculation results are sent to the salve controllers through the optical fibers. As the data transmission rate of the optical fibers is finite, the delay exists in the data transmission process. In this paper, this delay is denoted as $T_{d,net}$.

For the convenience to design the closed-loop controllers and to improve the system stability, generally, the sum of the computation delay $T_{d,ca}$ and the transmission delay $T_{d,net}$ is quantized as T_{ctr}, the effective control period. (In digital control chips, double registers are adopted by the modulating wave, including a compare register and a shadow register. The value of the compare register is compared with the carrier wave in every moment, and then the PWM driver signals are generated. Every new value of the modulating wave is stored into the shadow register first after being obtained by the slave controller. For AS-PWM, the shadow register is renewed in every control period T_{ctr}, and its value is loaded into the compare register when the corresponding carrier wave reaches its peak or valley.) In order to make each computation result take effect in PWM, it is generally chosen that $T_{ctr} > T_{d,ca} + T_{d,net}$. Combining with $T_{ctr} = T_{sw}/(2N)$, we get

$$T_{sw} > 2N \times (T_{d,ca} + T_{d,net})$$

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or $$f_{sw} < \frac{1}{2N \times \left(T_{d,ca} + T_{d,net}\right)} \quad (1)$$

It is indicated that for AS-PWM, there is an upper limit value to select the switching frequency f_{sw}. However, in general, the switching frequency f_{sw} is up to the switching losses and the maximum cooling capacity allowable. If the temperature rising of the semiconductor power devices and the power conversion efficiency can be controlled within an allowable range, it is inclined to increase the switching frequency. Because it is beneficial to reduce the volume and weight of the ac input filter. The upper limitation results in the below contradiction which cannot be reconciled easily: in the same ac input voltage and the same rated power, if the cell number N is larger, the rated power of each cell becomes smaller, then according to the efficiency and cooling capacity allowable, the switching frequency f_{sw} can be selected higher; however, as the increase of cell number N, the computation time $T_{d,ca}$ become longer, which results in a lower value of f_{sw} according to (1).

The above problem has been reported in [30] as well: as the control period of the PETT controller is 175 μs, the switching frequency f_{sw} of the CHB is up to the cell number N, that is, $f_{sw} = 1/(2NT_{ctr})$. For example, if $N = 7$, $f_{sw} = 408$ Hz; if $N = 8$, $f_{sw} = 357$ Hz; and if $N = 9$, $f_{sw} = 317$ Hz.

2) Long Modulator Delay

The model of AS-PWM can be approximately represented in Fig. 6. v_{ctr}^{d} is the *digital modulating wave* after executing the main control algorithms and processing the quantization, which updates itself with the frequency of $2Nf_{sw}$. v_{ctr}^{dj} is the *digital modulating wave* of Cell j ($j = 1,2,\cdots,N$), which updates itself with the frequency of $2f_{sw}$. v_{ctr}^{bj} is the *quantized boxcar modulating wave* of Cell j. As shown in Fig. 4, from v_{ctr}^{dj} to v_{ctr}^{bj}, the ZOH effect exists. This ZOH model is denoted as $G_h^a(s)$ with the dominating frequency of $2f_{sw}$. $G_h^a(s)$ is the so-call modulator delay as well, that is,

$$G_h^a(s) = \frac{2}{T_{sw}} \cdot \frac{1 - e^{-s(T_{sw}/2)}}{s} \approx e^{-s(T_{sw}/4)} \quad (2)$$

On the contrary, for MS-PWM, as all of the modulating waves are v_{ctr}^{b} (as shown in Fig. 5(b)), which update themselves with the frequency of $2Nf_{sw}$, the modulator delay (also the ZOH effect from v_{ctr}^{d} to v_{ctr}^{b}) is

$$G_h^b(s) = \frac{2N}{T_{sw}} \cdot \frac{1 - e^{-s(T_{sw}/2N)}}{s} \approx e^{-s(T_{sw}/4N)} \quad (3)$$

Compared $G_h^a(s)$ with $G_h^b(s)$, it can be found that there is long modulator delay in AS-PWM, which may seriously influence the dynamic response and the system stability, especially when the switching frequency is relatively low.

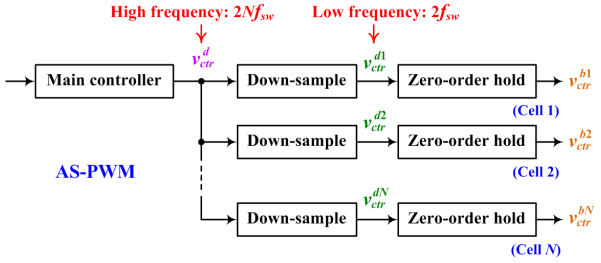

Fig. 6. The approximate model of AS-PWM.

The simulation results based on a five-cell PETT are exhibited in Fig. 7. In the simulation, the switching frequency of the CHB is $f_{sw} = 500$ Hz, and the control frequency is $f_{ctr} = 5$ kHz. With the same control algorithms and the same controller parameters, the simulation waveforms based on AS-PWM are shown in Fig. 7(a), while the simulation waveforms based on MS-PWM are shown in Fig. 7(b). It can be seen that based on AS-PWM, the system is instable, and the oscillation with large amplitude occurs in the dc output voltages in each CHB cell, v_{dcj} ($j = 1,2,\cdots,5$), and the ac input current, i_g. However, the system based on MS-PWM is stable. Due to the theme and the space limitation of this paper, the influence of the modulator delay on the system stability is not presented here, and similar researches can be found in [16]-[17].

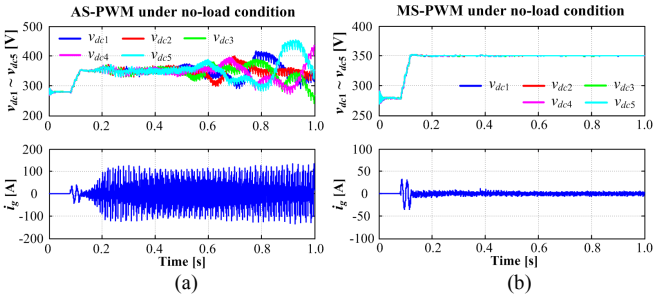

Fig. 7. The simulation waveforms based on a five-cell PETT. The switching frequency of the CHB is $f_{sw} = 500$ Hz, and the control frequency is $f_{ctr} = 5$ kHz. (a) Based on AS-PWM, the simulation waveforms of the dc output voltages in each CHB cell v_{dcj} ($j = 1,2,\cdots,5$) (Top) and the ac input current i_g (Bottom); (b) based on MS-PWM, the simulation waveforms of the dc output voltages in each CHB cell v_{dcj} ($j = 1,2,\cdots,5$) (Top) and the ac input current i_g (Bottom).

3) Aliasing Phenomenon towards the Digital Modulating Waves

As shown in Fig. 5(a) and Fig. 6, the updating frequency of v_{ctr}^{d} is $2Nf_{sw}$, and the updating frequency of v_{ctr}^{dj} (v_{ctr}^{bj}) is $2f_{sw}$. Therefore, from v_{ctr}^{d} to v_{ctr}^{dj}, there must be a down-sampling process, in which the dominating frequency is decreased. Taking v_{ctr}^{d1} as an instance, the relationship between v_{ctr}^{d1} and v_{ctr}^{d} in terms of the z-transform can be obtained as

$$V_{ctr}^{d1}(z) = \frac{1}{N}\sum_{k=0}^{N-1} V_{ctr}^{d}\left(z^{\frac{1}{N}} e^{-j\frac{2\pi k}{N}}\right) \quad (4)$$

where $V_{ctr}^{d1}(z)$ is the z-transform of $v_{ctr}^{d1}[k]$, $V_{ctr}^{d}(z)$ is the z-transform of $v_{ctr}^{d}[k]$, and $z = e^{sT_{sw}/2} = e^{s/2f_{sw}}$. The derivation of (4) is shown in Appendix. As $z = e^{s/2f_{sw}} = e^{j2\pi f/2f_{sw}} = e^{j\pi f/f_{sw}}$, we get

$$V_{ctr}^{d1}\left(e^{j\frac{\pi}{f_{sw}}f}\right) = \frac{1}{N}\sum_{k=0}^{N-1} V_{ctr}^{d}\left(e^{j\frac{\pi}{f_{sw}}\frac{f-k\cdot 2f_{sw}}{N}}\right) \quad (5a)$$

That is,

$$V_{ctr}^{d1}(f) = \frac{1}{N}\sum_{k=0}^{N-1} V_{ctr}^{d}\left(\frac{f - k\cdot 2f_{sw}}{N}\right) \quad (5b)$$

Based on (5b), it can be inferred that the amplitude-versus-frequency curve of v_{ctr}^{d1} can be generated from v_{ctr}^{d} through translation and scaling.

From the point of spectrum, as the dominating frequency of v_{ctr}^{d} is $2Nf_{sw}$, its baseband (or nyquist band) is $-Nf_{sw}$~Nf_{sw}.

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For the sake of analysis, the baseband is separated into two parts, which are denote as low-frequency components and high-frequency components. The maximum frequency of the low-frequency components is denoted as $f_{lw,max}$. Generally, in the whole baseband of v_{ctr}^{d}, the low-frequency components ($-f_{lw,max}\sim f_{lw,max}$) are abundant and the high-frequency components ($-Nf_{sw}\sim -f_{lw,max}, Nf_{sw}\sim f_{lw,max}$) with remarkable magnitude are rare. (In order to suppress the impact of low-frequency harmonics of v_g on i_g, there should be some low-frequency components contained in v_{ctr}^{d} with certain amplitude.) Hence, the influence of the high-frequency components can be neglected.

Taking $f_{sw} < f_{lw,max}$ as an instance, based on (5b), the spectrum of v_{ctr}^{d} and v_{ctr}^{d1} is shown in Fig. 8. After down-sampling v_{ctr}^{d}, aliasing occurs in the spectrum of v_{ctr}^{d1}, that is, the spectrum overlaps near the frequency of $\pm f_{sw}, \pm 3f_{sw}, \cdots$. It will make the line-current closed-loop controller lose its regulation effect, and deteriorate the ac input current i_g. Therefore, if providing that the high-frequency components play a very weak role in the aliasing phenomenon, it must satisfy the in-equation below

$$f_{sw} > f_{lw,max} \tag{6}$$

so that the spectrum aliasing towards v_{ctr}^{dj} can be avoided.

It means that for AS-PWM, there is a lower limit value when selecting the switching frequency.

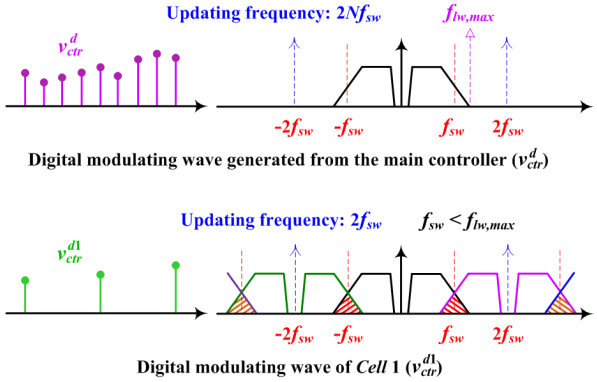


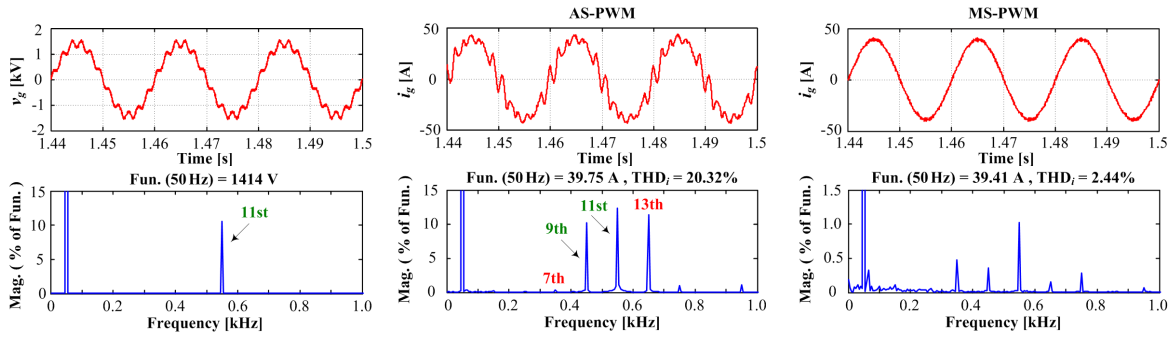
Fig. 8. For AS-PWM, the spectrum of v_{ctr}^{d} and v_{ctr}^{d1}, where $f_{sw} < f_{lw,max}$ and the spectrum aliasing occurs for v_{ctr}^{d1}.

In Fig. 7, the system is unstable. On this basis, the proportionality coefficient of the line-current closed-loop controller is reduced to 1/3 of the original one. In this case, whether adopting AS-PWM or adopting MS-PWM, the system is always stable (the gain cross-over frequency is decreased while the phase margin is increased, but the amplitude-frequency characteristic of the open-loop transfer function is still the same in AS-PWM based system and MS-PWM based system). The simulation results based on a five-cell PETT is exhibited in Fig. 9.

From Fig. 9(a), there is 11st-order (550 Hz) harmonic component contained in v_g, which is higher than the switching frequency $f_{sw} = 500$ Hz. In order to suppress the impact of v_g on i_g, 11st-order harmonic controller is enabled in the ac-input-current regulator ($G_{ci}(z)$ as shown in Fig. 12), and 11st-order harmonic with certain magnitude exists in v_{ctr}^{d}. According to the indication in Fig. 8, if the spectrum overlaps near the frequency of $\pm f_{sw}$, the amplitude of the 11st-order harmonic component contained in v_{ctr}^{d1} is different with the one contained in v_{ctr}^{d} (which make the ac-input-current regulator lose its suppression effect to the 11st-order harmonic), and v_{ctr}^{d1} will contain the 9th-order harmonic component with quite large magnitude. Therefore, it can be predicted that remarkable 9th-order and 11st-order harmonics may exist in the ac input current i_g if AS-PWM is applied. On the contrary, as there is no down-sample process in MS-PWM, the 11st-order harmonic controller will play its role and eliminate the 11st-order harmonic in i_g.

With the same control algorithms and the same controller parameters, the simulation waveforms based on AS-PWM are shown in Fig. 9(b), and the simulation waveforms based on MS-PWM are shown in Fig. 9(c). The simulation results are almost consistent to the above prediction. For AS-PWM, as shown in Fig. 9(b), there are remarkable 9th-order (450 Hz), 11st-order (550 Hz) and 13th-order (650 Hz) harmonics contained in i_g. For MS-PWM, as shown in Fig. 9(c), the 9th-order and11st-order harmonics contained in i_g have small magnitude.

Besides, as for the 13th-order harmonic shown in Fig. 9(b), it generates from the dead time and the aliasing effect. In the simulation, the dead time is set as $T_{dead} = 6$ μs. And some odd harmonics contained in i_g may generate. Through the feedback control, such odd harmonics appear in v_{ctr}^{d}. Due to the aliasing effect, some harmonics, such as 13th-order harmonic, may be amplified in v_{ctr}^{d} and deteriorate i_g.



(a) (b) (c)

Fig. 9. The simulation waveforms based on a five-cell PETT. The switching frequency of the CHB is $f_{sw} = 500$ Hz, and the control frequency is $f_{ctr} = 5$ kHz. (a) The ac input voltage v_g (Top) and its spectrum (Bottom); (b) based on AS-PWM, the ac input current i_g (Top) and its spectrum (Bottom); (c) based on MS-PWM, the ac input current i_g (Top) and its spectrum (Bottom).

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As analyzed above, based on AS-PWM, the effective control period is chosen as $T_{ctr} = T_{sw}/(2N)$ for a N-cell CHB. It can ensure each computation result playing its role in PWM, as shown in Fig. 5(a). However, in some application, the control period may be larger or smaller than $T_{sw}/(2N)$. For the larger one, some computation result may take effect twice (or even many times) in PWM (a little like the situation shown in Fig. 10(a)). For the smaller one, some computation result may lose its effect in PWM [36] (a little like the situation shown in Fig. 10(b)). Anyhow, the problems towards the long modulator delay and the spectrum aliasing still exist. They root in the implementation scheme of AS-PWM, where the modulating wave in each cell updates itself when its corresponding carrier reaches its peak and valley. For avoiding confusion, in this paper, the AS-PWM technique with control period of $T_{sw}/(2N)$ is focused on.

To sum up, there are three problems suffered by AS-PWM, including the upper limitation of the switching frequency, the long modulator delay and the spectrum aliasing towards the *digital modulating waves*, which may restrict the application of AS-PWM in the low-switching-frequency and multi-cell system. (However, it should be noticed that AS-PWM is still effective in some application where the switching frequency f_{sw} is high, the control frequency f_{ctr} is set the same value as the updating frequency (f_{ud}) of each modulating wave (for example, $f_{ctr} = f_{ud} = 2f_{sw}$ [34]), and the computation time $T_{d,ca}$ and data transmission time $T_{d,net}$ are small. In such application, there is no down-sampling effect in PWM and the modulator delay is normal.) Hence, it is recommended to adopt MS-PWM whose basic principle is shown in Fig. 5(b). In MS-PWM, all of the modulating wave update themselves at the same time, and there is no down-sampling effect in each cell. For MS-PWM, the updating frequency of the modulating wave can be chosen as different values. For example, when $N = 2$, the updating frequency can be selected as $4f_{sw}$, as shown in Fig. 5(b); the updating frequency can be selected as $2f_{sw}$, as shown in Fig. 10(a); the updating frequency can be selected as $8f_{sw}$, as shown in Fig. 10(b). As for the extra pulses, the basic idea to eliminate them is briefly introduced in Appendix.

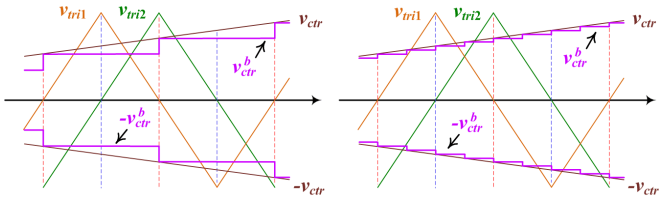

Fig. 10. Based on MS-PWM. (a) The updating frequency of the modulating wave is $T_{sw}/2$; and (b) the updating frequency of the modulating wave is $T_{sw}/8$.

IV. Multirate Technique for the CHB Converter

In MS-PWM, the control frequency f_{ctr} is irrelevant to the switching frequency f_{sw}. In this case, if the control frequency f_{ctr} is still selected according to $f_{ctr} = 2Nf_{sw}$ (before selecting f_{ctr}, f_{sw} has been chosen), the advantages of MS-PWM cannot be made full use of. In other words, for MS-PWM, it can select f_{ctr} purely on the basis of computation delay $T_{d,ca}$ and transmission delay $T_{d,net}$ without considering f_{sw}. For some application such as the PETT, $T_{d,ca}$ and $T_{d,net}$ are quite long, and hence, it is hard to select a relatively high value of f_{ctr}.

The control frequency f_{ctr} (or the delay $T_{d,ca}$ and $T_{d,net}$) is closely bound up to the control performance of power electronic converters. In the past decades, there are two different ways to improve the control performance. The first way is more direct and from the point of control, including the modification and development of control strategies. The typical example is the model predictive control [9]-[11]. However, even for such high-performance control strategies like the predictive control, it still needs to spend one or several control periods ($T_{ctr} = 1/f_{ctr}$) to make the real value completely follow the reference. The second way is indirect and from the point of signal processing, including the anti-aliasing sampling, the minimization of time delay and so on. For example, by reducing the computation delay, the steady-state performance, the dynamic response and the system stability can be improved [9], [12]-[17]. The research presented in this paper follows the second way.

As the digital chips (hardware) in a PETT is organized as a distributed structure, the algorithms (software) can also adopt a distributed structure and can be separated into three parts, including the sampling, control and modulation, which can be executed in different digital chips. Through the better matching between the distributed hardware and the distributed software, high efficient utilization of digital chips and good control performance of the PETT can be achieved at the same time. In a word, it is necessary and beneficial to separate the sampling frequency f_{sa}, control frequency f_{ctr} and modulating-wave updating frequency f_{ud} from the switching frequency f_{sw}, following with independently selecting the values of f_{sa}, f_{ctr} and f_{ud}. This is the so-call multirate concept presented in this paper. In this section, a universal-type multirate structure for the CHB is proposed. On this basis, a simplified structure is proposed. And then the selection principles of f_{sa}, f_{ctr} and f_{ud} are introduced, following with the presentation of the basic principles of up-sampling and interpolation filtering.

A. Multirate Structures for the CHB

In the following paper, a universal-type multirate structure for the CHB is introduced at first, which is shown in Fig. 11(a). On this basis, the simplified structure is exhibited in Fig. 11(b). In Fig. 11, $DecFlt(z)$ and $ItpFlt(z)$ are the decimation filter and the interpolation filter respectively, which are all the low-pass filters. The basic principle of down-sampling and decimation filtering is introduced in the part *B* of Section III, while the basic principle of up-sampling and interpolation filtering is introduced in the part *C* of this section.

In Fig. 11(a), the sampling frequency of v_g and i_g ($f_{sa,ac}$) is M times of the control frequency f_{ctr} (where $M > 1$ but M may not be an integer), the sampling frequency of v_{dcj} ($f_{sa,dc}$) is the same as f_{ctr}; v_{dcj} is sampled by the slave controller and the sample data are transmitted to the main controller through the optical fibers, while v_g and i_g are sampled by the main controller without data transmission; the modulating-wave updating frequency f_{ud}^1 is L times of f_{ctr}; the new computation result of the modulating wave is received by the slave controller and stored into a register, and then the modulating wave is up-sampled and interpolated with the use of stored data.

For the universal-type structure shown in Fig. 11(a), *Double*

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Register 1 and *Double Register* 2 all represent the quantization of time delay. For *Double Register* 1, the datum received by the slave controller is stored into the first register, and then the value of the first register is loaded into the second register with the frequency of f_{ctr}. For *Double Register* 2, the datum after interpolation filtering is stored into the first register, and then the value of the first register is loaded into the second register with the frequency of f_{ud}^1. (For *Double Register* 2, the first register is also the PWM shadow register, while the second register is also the PWM compare register.) *Double register* 1 represents the quantization of the computation time of down-sampling and decimation filtering ($T_{d,ca}^1$), the computation time of executing the main control algorithms ($T_{d,ca}^0$) and the data transmission time ($T_{d,net}$), that is, $T_{ctr} > T_{d,ca}^1 + T_{d,ca}^0 + T_{d,net}$, where $T_{ctr} = 1/f_{ctr}$. *Double register* 2 represents the quantization of the computation time of up-sampling and interpolation filtering ($T_{d,ca}^2$), that is, $T_{ud}^1 > T_{d,ca}^2$, where $T_{ud}^1 = 1/f_{ud}^1$.

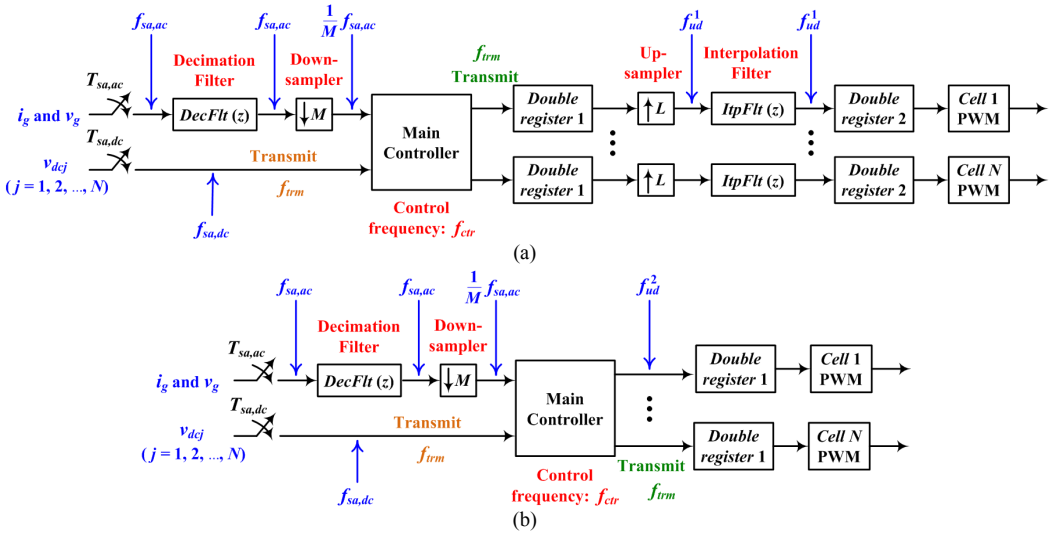

Fig. 11. The proposed multirate structures of the CHB: (a) the universal-type structure, and (b) the simplified structure.

Then,

$$\frac{f_{sa,ac}}{M} = f_{sa,dc} = f_{ctr} = f_{trm} = \frac{f_{ud}^1}{L} \tag{7}$$

In the universal-type structure, the frequencies $f_{sa,ac}$ and f_{ud}^1 are relatively high while the frequency f_{ctr} is relatively low, which is consistent with the time-resource occupation of the sampling, control and modulation. Combining with Fig. 2, specifically speaking, the main control algorithms are executed in the DSP of the main controller; the sampling, decimation filtering and down-sampling of v_g and i_g are achieved in the FPGA and DSP of the main controller; the sampling of v_{dcj} is achieved in the FPGA and DSP of the slave controller; the up-sampling and interpolation filtering of the modulating wave are achieved in the FPGA and DSP of the slave controller. Compared with the situation where the frequencies $f_{sa,ac}$, f_{ctr} and f_{ud}^1 are set as the same value, with the same control frequency f_{ctr}, the quality of i_g can be further improved by the proposed multirate structure. The detailed mechanism is presented in the next part.

The structure shown in Fig. 11(b) is a simplified version of the universal-type one. In this simplified structure, there is no interpolation towards the modulating waves, and the modulating-wave updating frequency f_{ud}^2 is the same as the control frequency f_{ctr}. Compared with the universal-type structure, the total time delay of the simplified version is much smaller (there is some phase lag in the interpolation filter, and *Double register* 2 doesn't exist in the simplified structure), which results in faster dynamic response. Hence, in some application which has high requirement on the system dynamic performance, the simplified structure can be adopted. Detail information about the simplified structure can be referenced in [37], where the simplified structure is briefly indicated in the PETT level with the noise suppression technique and voltage balance control strategy.

In order to more clearly expound the proposed multirate technique, the CHB's control system based on the universal-type structure in z-transform is exhibited in Fig. 12. v_g is the ac input voltage, i_g is the ac input current, and v_{dcj} is the dc voltage of Cell j, where $j = 1,2,\cdots,N$. The sampling frequency of v_g and i_g is f_{sa_ac}, where f_{sa_ac} is higher than f_{ctr}, the control frequency. After sampling v_g and i_g, the sampling data are processed by a decimation filter, which is denoted as $DecFlt(z)$, and then are down-sampled to obtain new data with dominating frequency of f_{ctr}, where $f_{sa\_ac} = Mf_{ctr}$. The sampling frequency of v_{dcj} is f_{sa_dc}, which is equal to f_{ctr}. The sampling, filtering and down-sampling of v_g and i_g are executed in the main controller, while the sampling of v_{dcj} is executed in each salve controller and then sent to the main controller through the optical fibers.

$G_{cv}(z)$ is the dc-voltage regulator, $G_{ci}(z)$ is the ac-input-current regulator, PLL is the phase locked loop, $F_{avg}(z)$ is the moving-average filter which aimed at filtering the second-order component contained in the dc voltages. They are all executed in the main controller, and their dominating frequencies are all equal to f_{ctr}.

The computation result (v_{ctr}) is sent to each salve controller through the optical fibers. The datum received by the salve controller is stored into a register first. Then, at each certain

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time, the stored datum is loaded into another register, following with being up-sampled and filtered by $ItpFlt(z)$, the interpolation filter. Here, the storing-and-loading effect is denoted as *Double register* 1, and its z-transform is z^{-1}, where the dominating frequency is f_{ctr} (that is, $z = e^{sT_{ctr}}, T_{ctr} = 1/f_{ctr}$). The dominating frequency of $ItpFlt(z)$ is f_{ud}^1, the updating frequency of modulating waves, where $f_{ud}^1 = Lf_{ctr}$. After being filtered, with similar principle, the new datum is stored into the PWM shadow register first and then loaded into the PWM compare register. This effect is denoted as *Double register* 2, and its z-transform is z^{-1}, where the dominating frequency is f_{ud}^1 (that is, $z = e^{sT_{ud}^1}, T_{ud}^1 = 1/f_{ud}^1$).

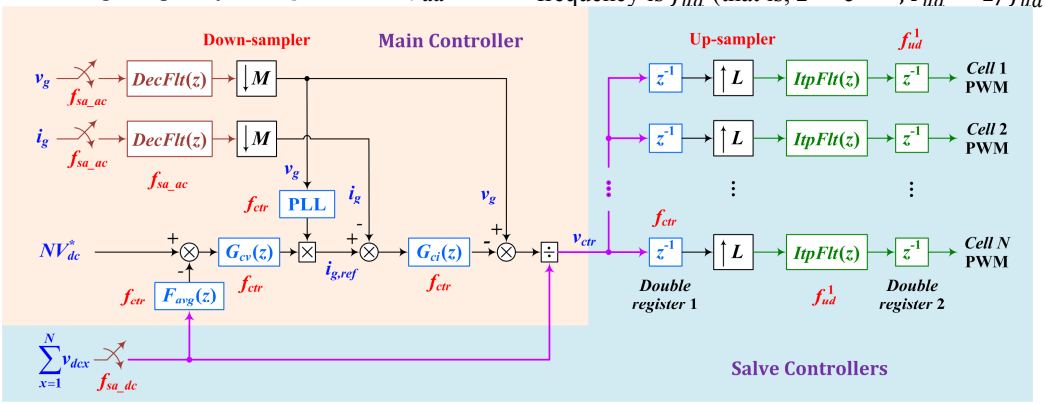

Fig. 12. The control system of the CHB based on the proposed universal-type multirate structure.

B. Selection Principles of Sampling Frequency, Control Frequency and Modulating-Wave Updating Frequency

In this paper, the selection principles of sampling frequency f_{sa}, control frequency f_{ctr} and modulating-wave updating frequency f_{ud} will be introduced respectively.

1) *Sampling Frequency*

For the sampling frequency of i_g, its selection principle is relevant with the carrier-based PWM technique, the total cell number N and the balance control strategy. In order to sample the low-frequency components of i_g without distortion as far as possible and avoid the adoption of anti-aliasing analog pre-filters, it needs to synchronize the PWM and the sampling, and to choose suitable sampling instants to make each of them near to the arithmetic average of two adjacent switching times [9]. If the PS-PWM technique and the voltage balance control strategy proposed in [26] are adopted, the equivalent switching frequency of i_g is $2Nf_{sw}$ and the sampling frequency of i_g can be selected as

$$f_{sa,ac}^1 = Q_1 \times f_{sw} \tag{8}$$

where Q_1 is the common divisor of $4N$, and $Q_1 = 1,2,\cdots,4N$. For this case, the highest value of the sampling frequency is $max(f_{sa,ac}^1) = 4Nf_{sw}$.

As shown in Fig. 3, due to $L_s \neq 0$ in practice, the high-frequency harmonics of i_g will be coupled to v_g through L_s [31]. In general, v_g is sampled by the PETT digital control system and used for phase locking and other control. The waveforms of i_g, v_{Ls} and v_g are shown in Fig. 13(a). v_{Ls} is the voltage of L_s. According to the sampling principle of i_g, it cannot be avoided to sample the high-frequency components of v_g. Therefore, the sampling and signal processing scheme of v_g is proposed as below:

The sampling frequency of v_g can be selected as

$$f_{sa,ac}^2 = \frac{4Nf_{sw}}{Q_2}(Q_2 = 1,3,5,\cdots) \quad \text{and} \quad f_{sa,ac}^2 \geq f_{ctr} \tag{9}$$

After being sampled, the data are processed by a digital low-pass filter to remove the high-frequency components and reserve the low-frequency components. Then, the signal is down-sampled. In practice, the above low-pass filter is a decimation filter as well.

Synthesizing the sampling principles of v_g and i_g, for convenience, it can set $f_{sa,ac}^1$ and $f_{sa,ac}^2$ as the same value, that is, $f_{sa,ac} = f_{sa,ac}^1 = f_{sa,ac}^2 = 4Nf_{sw}$. Besides, the same decimation filter ($DecFlt(z)$) is adopted after sampling v_g and i_g.

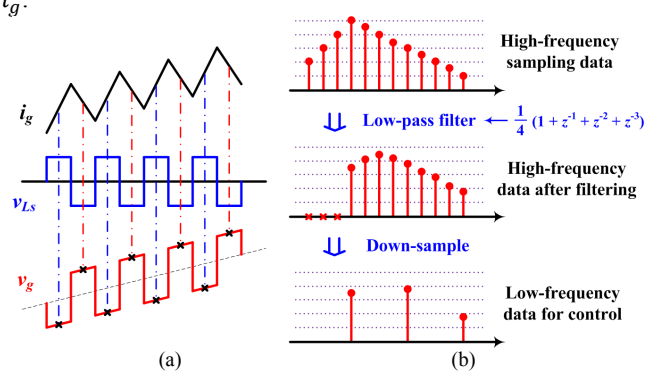

Fig. 13. (a) The waveforms of i_g, v_{Ls} and v_g; (b) taking the moving average filter as an instance, sample with high frequency, filter and down-sample.

Increasing the sampling frequency $f_{sa,ac}$ is beneficial to improve the quality of i_g. The main reasons are indicated as follows.

Firstly, in the sampling process of i_g, actually, it is hard to make every sampling point stay in the midpoint of the switching ripple of i_g, especially when i_g passes zero. In other words, the spectrum aliasing may occur in sampling i_g. From the point of spectrum, in order to reduce the aliasing impact as far as possible, it should improve the sampling frequency of i_g, and make the aliasing size between the baseband and other adjacent frequency bands as small as possible. It is similar to the analysis related to Fig. 9.

Secondly, as shown in Fig. 11 and Fig. 13(b), after sampling i_g with high frequency, the sampling data should be processed by a low-pass filter, and then be down-sampled. In this case, the

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low-pass filter plays several roles. For example, the high-frequency data are weighted by the low-pass filter so that one single low-frequency datum after down-sampling can represent multiple high-frequency data before filtering, which can make the controller $G_{ci}(z)$ regulate i_g well. For the sake of analysis, the moving-average filter is taken as an instance to indicate the above mechanism in Fig. 13(b).

2) *Control Frequency*

As the execution of control algorithms cannot be achieved in an instant, certain calculation time is needed, which is noted as $T_{d,ca}$ (the computation delay). As shown in Fig. 2, the calculation results acquired by the main controller will be sent to each slave controller through optical fibers. And the data transmission based on optical fibers also spends time, which is noted as $T_{d,net}$ (the transmission delay). The control period T_{ctr} should be larger than the sum of $T_{d,ca}$ and $T_{d,net}$. Otherwise, some calculation results will lose their effect, and the main controller will lose its control ability at those moments.

However, choosing a low control frequency is unwise, because it may seriously worsen the control performance. It is an important control objective of the CHB to eliminate the low-frequency harmonic components of i_g as far as possible. In general, harmonic controllers to support the cancellation of low-frequency harmonics are needed in the controller $G_{ci}(z)$ [30], [32]. In order to make them work, the maximal frequency of those low-frequency harmonics needed to be cancelled ($f_{lw,max}$) should be less than $f_{ctr}/2$, that is, $f_{ctr} > 2f_{lw,max}$. Therefore,

$$2f_{lw,max} < f_{ctr} < \frac{1}{T_{d,ca} + T_{d,net}} \tag{10}$$

3) *Modulating-Wave Updating Frequency*

Different with the sampling frequency and the control frequency, the modulating-wave updating frequency f_{ud} should be as high as possible. The considerations are as follows:

Firstly, there is a quantization process when the new calculation result of the modulating wave generated from the main controller is prepared to send to the slave controller. In this process, the modulating wave with floating-point form is transformed to a new integer one with fix-point form. The quantization will bring some noise into the control system. In [33], it is shown that with higher value of f_{ud}, it is beneficial to weaken the quantization effect. However, for our application where the switching frequency is quite low, as the quantized modulating wave always has high resolution (the word length is 16-bit generally), the benefit to increase f_{ud} just for quantization issue is not remarkable.

Secondly, as indicated in Section III, for MS-PWM, the transfer function from *digital modulating wave* v_{ctr}^d to the *quantized boxcar modulating wave* v_{ctr}^b can be represented by the ZOH model $G_h^b(s)$. The dominating frequency of $G_h^b(s)$ is equal to the modulating-wave updating frequency f_{ud}. The spectrum of v_{ctr}^d and v_{ctr}^b, and the amplitude-versus-frequency curve of $G_h^b(s)$ are shown in Fig. 14. v_{ctr}^d is a digital signal. Its baseband is $-0.5f_{ud}$~$0.5f_{ud}$, and the spectrum of the baseband is repeated in the whole frequency band with the period of f_{ud} [28]. As shown in Fig. 14, for v_{ctr}^b, harmonics with remarkable magnitude exist near the frequency of f_{ud}. Notice that such harmonics are different with PWM sideband harmonics, and there is no relationship between such harmonics and the modulation process. They cannot be eliminated by adopting PS-PWM. For the sake of denoting, such harmonics are named as digital-to-analog high-frequency harmonics with the abbreviation of D/A HF-harmonics. The spectrum of the PWM voltage v_{conv} is closely bound up to v_{ctr}^b, and the harmonics of v_{conv} will be coupled to i_g through the ac input filter inductor L_g. Therefore, as the increasing of f_{ud}, the D/A HF-harmonics contained in v_{conv} will be shifted to a higher-frequency zone. In this case, under the attenuation effect of $(1/sL_g)$, the amplitude of the D/A HF-harmonics contained in i_g will become smaller.

Thirdly, as shown in Fig. 14, with the increasing of f_{ud}, the amplitude of $G_h^b(s)$ in the low-frequency band will be much closer to 1, which will make v_{ctr}^b much more similar to v_{ctr}^d. In order to weaken the impact of the low-frequency harmonics of v_g and the dead time of IGBTs, harmonic controllers are generally needed in $G_{ci}(z)$ [30], [32]. Harmonic controllers play their role through v_{ctr}^d, v_{ctr}^b and v_{conv}. Therefore, if the amplitude of v_{ctr}^b in the low-frequency band is totally the same as the one of v_{ctr}^d, the harmonics cancellation will become more succeeded and the quality of i_g will be improved significantly.

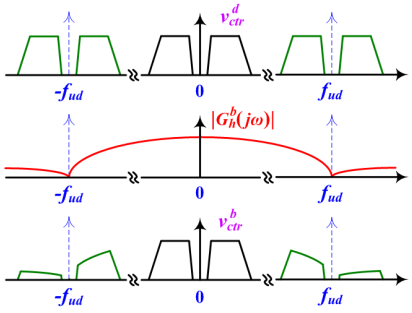

Fig. 14. The spectrum of the digital modulating wave v_{ctr}^d and the quantized boxcar modulating wave v_{ctr}^b, and the amplitude-versus-frequency curve of the ZOH model $G_h^b(s)$.

Synthesize the above analyses, the advantages to separate the sampling frequency $f_{sa,ac}$, the control frequency f_{ctr} (the data transmission frequency f_{trm}) and the modulating-wave updating frequency f_{ud} can be concluded as follow:

1) It can choose a higher sampling frequency $f_{sa,ac}$ to precisely acquire the information of signals being sampled;

2) It can choose a higher modulating-wave updating frequency f_{ud} to improve the control effect of the inner line current controller and further attenuate the D/A HF-harmonics;

3) It can choose a relatively low control frequency f_{ctr} (data transmission frequency f_{trm} as well) to increase the time margin of calculation and reduce the time occupation of data transmission.

C. Basic Principle of Up-Sampling and Interpolation Filtering

The principle of up-sampling and interpolation process is shown in Fig. 15. For the sake of analysis, the input signal of the up-sampler is denoted as $x_{in}[n]$ (whose dominating frequency is f_{ctr}), the output signal of the up-sampler is denoted as $x_{out}[n]$ (whose dominating frequency is $f_{ud} = Lf_{ctr}$), and the output signal of $ItpFlt(z)$ is denoted as $y_{itp}[n]$

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(whose dominating frequency is $f_{ud} = Lf_{ctr}$). The up-sampler works like that: between every two adjacent samples of $x_{in}[n]$, $(L-1)$ zero-valued samples are inserted equidistantly to obtain $x_{out}[n]$. That is,

$$x_{out}[n] = \begin{cases} x_{in}[n/L], & n = 0, \pm L, \pm 2L, \cdots, \\ 0, & \text{otherwise.} \end{cases} \quad (11)$$

Then,

$$X_{out}(z) = \sum_{n=-\infty}^{+\infty} x_{out}[n] z^{-n} = X_{in}(z^L) \quad (12)$$

where $z = e^{sT_{ud}}$, $T_{ud} = 1/f_{ud}$ and $f_{ud} = Lf_{ctr}$. Hence,

$$X_{out}\left(e^{j2\pi \frac{f}{f_{ud}}}\right) = X_{in}\left(e^{j2\pi \frac{Lf}{f_{ud}}}\right)$$

or

$$X_{out}(f) = X_{in}(Lf) \quad (13)$$

Based on (13), the spectrum of $x_{out}[n]$ can be obtained, as shown in Fig. 15(b).

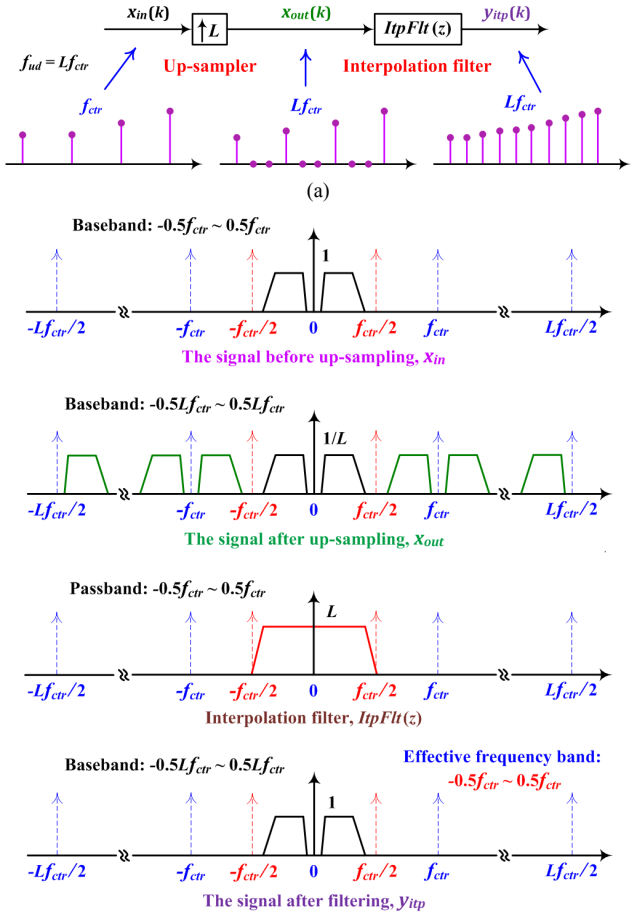

Fig. 15. (a) The principle of up-sampling and interpolation process, (b) the spectrum of the signals x_{in}, x_{out} and y_{itp}, and the amplitude-versus-frequency of $ItpFlt(z)$.

As shown in Fig. 15(b), in terms of $y_{itp}[n]$, the components staying in the frequency band of $(-Lf_{ctr}/2 \sim -f_{ctr}/2)$ and $(f_{ctr}/2 \sim Lf_{ctr}/2)$ are undesired, and should be filtered by the interpolation filter, $ItpFlt(z)$. Hence, $ItpFlt(z)$ should be designed as a low-pass filter, which can effectively attenuate harmonics stayed in the above frequency band. The design procedure of low-pass filters can be referred in [28].

V. Experiment Verification

Experiment results shown below is based on a five-cell PETT laboratory prototype with rated power of 30 kW. The topology of the laboratory prototype is shown in Fig. 16, where the DC/DC converters aren't exhibited.

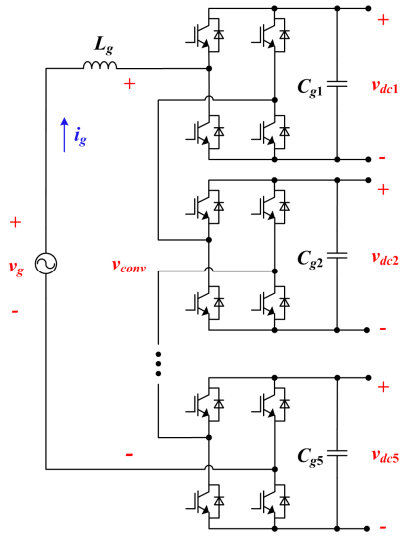

Fig. 16. The topology of the five-cell PETT laboratory prototype which is rated at 30 kW, where the DC/DC converters aren't exhibited.

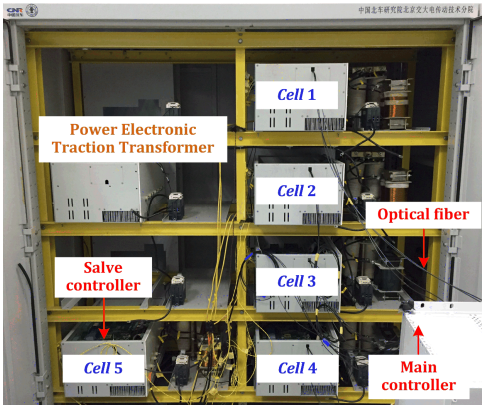

Fig. 17. The picture of the five-cell PETT laboratory prototype.

TABLE I
SYSTEM PARAMETERS OF THE CHB

Symbol	Quantity	Value
v_g	ac input voltage	1000 V/50 Hz
v_{dcj}	dc output voltages of each cell	350 V
L_g	ac input filter inductor	5 mH
C_{gj}	dc output capacitors of each cell	6.8 mF ± 20%
f_{sw}	switching frequency of the CHB	500 Hz
T_{dead}	dead time of the IGBTs	6 μs

In Fig. 16, L_g is the ac input filter inductor of the PETT, C_{gj} is the dc capacitor of Cell j; v_{dcj} is the dc voltage of Cell j, where $j = 1,2,\cdots,5$; v_g, i_g and v_{conv} are the ac input voltage, ac input current (or the line current) and PWM voltage of the

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PETT respectively. The picture of the laboratory prototype is shown in Fig. 17. The system parameters of the CHB are exhibited in Table I. In the experiment, the voltage balance is achieved by the output-parallel DC/DC converters [26], and all of the experiment results are based on the resistive load.

A. Comparison between AS-PWM and MS-PWM

As the cell number of the CHB is $N = 5$, the sampling frequency, control frequency, modulating-wave updating frequency and data transmission frequency can be set as 5 kHz uniformly, that is, $f_{sa,ac} = f_{sa,dc} = f_{ctr} = f_{ud} = f_{trm} =$ 5 kHz. With the same algorithms and the same parameters, the experiment waveforms based on AS-PWM are shown in Fig. 18(a), and the experiment waveforms based on MS-PWM are shown in Fig. 18(b).

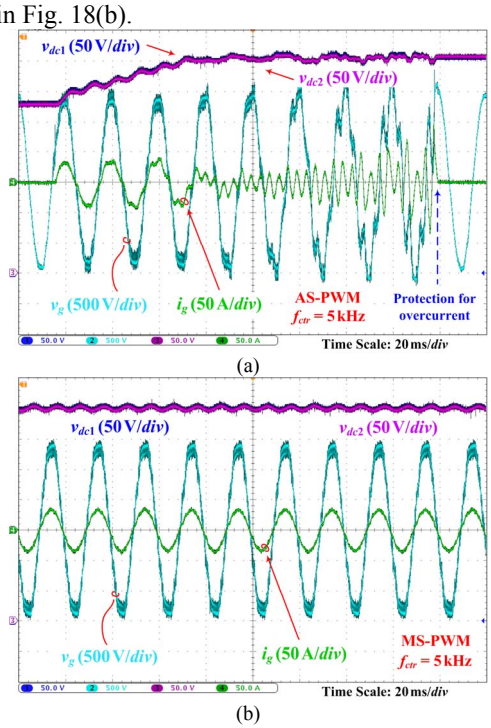
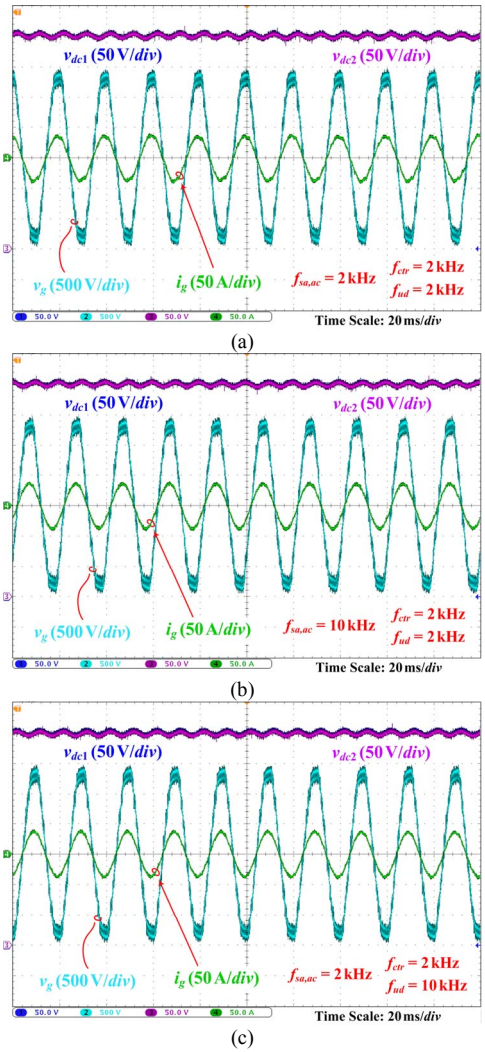


Fig. 18. Experiment results about the comparison between AS-PWM and MS-PWM. (a) The CHB is under no-load condition and AS-PWM is adopted. The experiment waveforms of the dc voltage of Cell 1-2, v_{dc1} and v_{dc2}, the ac input voltage v_g and the ac input current i_g. (b) The CHB is under heavy-load condition and MS-PWM is adopted. The experiment waveforms of the dc voltage of Cell 1-2, v_{dc1} and v_{dc2}, the ac input voltage v_g and the ac input current i_g

As shown in Fig. 18(a), after the CHB starts (the CHB is still under no-load condition), serious oscillation occurs in i_g and finally leads to the protection and shutdown of the PETT. (The waveforms are consistent to the ones shown in Fig. 7(a), where Time < 0.2 s.) It means that the system stability is worsened when AS-PWM is adopted. On the contrary, as shown in Fig. 18(b), the CHB is stable all the time, and near-sinusoidal waveform of i_g is achieved under heavy-load condition. It means that the system stability can be maintained when MS-PWM is adopted. The experiment results are consistent to the theoretical analysis shown in Section III. However, as the ac input of the PETT is directly connected to the ac power supply of the laboratory, the harmonics of v_g cannot be altered (or controlled), and there is few harmonics with frequency higher than f_{sw} contained in v_g. In this case, the influence of the spectrum aliasing is weak, and the quality of i_g in MS-PWM based system is only a bit better than that in AS-PWM based system. Much stronger comparison towards spectrum aliasing in experiment is left for future research.

B. Quality of the Ac Input Current with Different Values of Sampling Frequency and Modulating-Wave Updating Frequency

MS-PWM is adopted. The sampling frequency of dc-side voltages, the control frequency and the data transmission frequency are set as 2 kHz uniformly, that is, $f_{sa,dc} = f_{ctr} = f_{trm} = 2$ kHz. With the same algorithms and the same parameters, the experiment waveforms when the sampling frequency $f_{sa,ac}$ and the modulating-wave updating frequency f_{ud} are set as different values are shown in Fig. 19. Among them, when $f_{sa,ac} = 2$ kHz and $f_{ud} = 2$ kHz, the experiment waveforms are shown in Fig. 19(a); when $f_{sa,ac} = 10$ kHz and $f_{ud} = 2$ kHz, the experiment waveforms are shown in Fig. 19(b); when $f_{sa,ac} = 2$ kHz and $f_{ud} = 10$ kHz, the experiment waveforms are shown in Fig. 19(c); when $f_{sa,ac} = 10$ kHz and $f_{ud} = 10$ kHz, the experiment waveforms are shown in Fig. 19(d).



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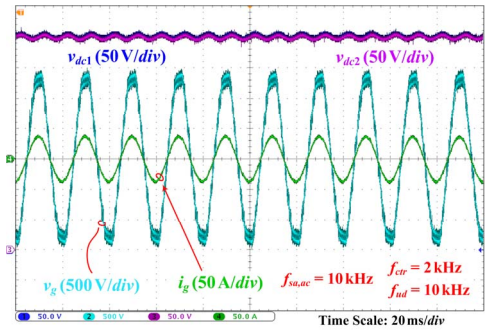

(d)

Fig. 19. Experiment results when the sampling frequency $f_{sa,ac}$ and the modulating-wave updating frequency f_{ud} are set as different values. The CHB is under heavy-load condition. MS-PWM is adopted. The experiment waveforms of the dc voltage of Cell 1-2, v_{dc1} and v_{dc2}, the ac input voltage v_g and the ac input current i_g. (a) $f_{sa,ac}$ = 2 kHz and f_{ud} = 2 kHz; (b) $f_{sa,ac}$ = 10 kHz and f_{ud} = 2 kHz; (c) $f_{sa,ac}$ = 2 kHz and f_{ud} = 10 kHz; (d) $f_{sa,ac}$ = 10 kHz and f_{ud} = 10 kHz.

Based on the data of i_g which are obtained from the experiment, the spectrum and the THD values (THD_i) of i_g are shown in Fig. 20(a) ~ Fig. 20(d). For clarity, the THD values (THD_i) and the amplitude values of i_g are collectively exhibited in Table II.

As shown in Fig. 19(a), Fig. 20(a) and Table II, when $f_{sa,ac}$ = 2 kHz and f_{ud} = 2 kHz, THD_i = 6.5996%. From Fig. 20(a), in term of the spectrum of i_g, the magnitude of 3rd-order (150 Hz) harmonic < the magnitude of 5th-order (250 Hz) harmonic < the magnitude of 7th-order (350 Hz) harmonic. As analyzed in the part *B* of Section IV, the mechanism is indicated as follows:

1) The information of different harmonic components acquired by the sampling process is different. The sampling accuracy of 3rd-order harmonic > the sampling accuracy of 5th-order harmonic > the sampling accuracy of 7th-order harmonic, which leads to different compensation effect to different harmonic components.

2) The attenuation of the ZOH $G_h^b(s)$ to different harmonic components contained in the *digital modulating wave* v_{ctr}^d is different. As shown in Fig. 13, the attenuation to 3rd-order harmonic of v_{ctr}^d < the attenuation to 5th-order harmonic of v_{ctr}^d < the attenuation to 7th-order harmonic of v_{ctr}^d. As a result, the 3rd-order harmonic content < the 5th-order harmonic content < the 7th-order harmonic content contained in the ac input current i_g.

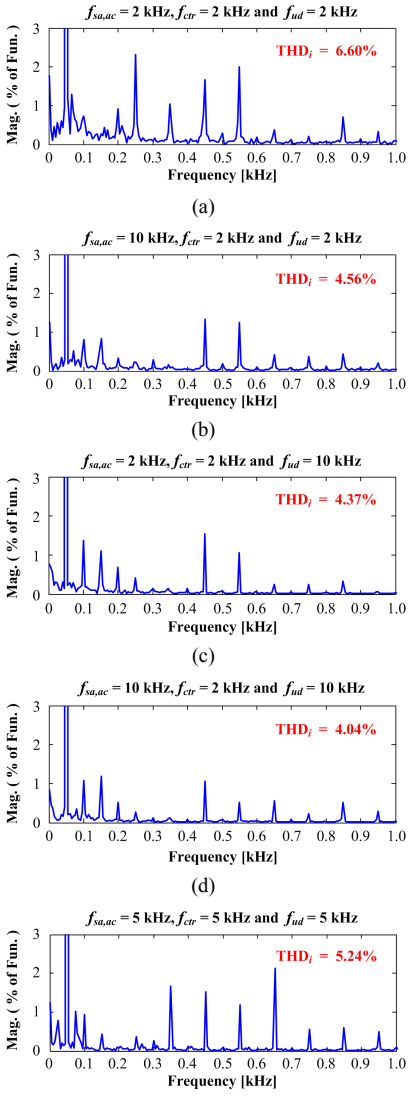

Fig. 20. The spectrum and the THD value of the ac input current i_g when the sampling frequency $f_{sa,ac}$, the control frequency f_{ctr} and the modulating-wave updating frequency f_{ud} are set as different values. The CHB is under heavy-load condition. MS-PWM is adopted.

TABLE II
THE THD VALUES AND THE AMPLITUDE VALUES OF THE AC INPUT CURRENT IN EXPERIMENT

	$f_{sa,ac}$ = 2 kHz f_{ctr} = 2 kHz f_{ud} = 2 kHz	$f_{sa,ac}$ = 10 kHz f_{ctr} = 2 kHz f_{ud} = 2 kHz	$f_{sa,ac}$ = 2 kHz f_{ctr} = 2 kHz f_{ud} = 10 kHz	$f_{sa,ac}$ = 10 kHz f_{ctr} = 2 kHz f_{ud} = 10 kHz	$f_{sa,ac}$ = 5 kHz f_{ctr} = 5 kHz f_{ud} = 5 kHz
Magnitude of the fundamental component (A)	36.3639	36.2492	36.2187	36.1559	33.4824
THD value of ac input current (%)	6.5996	4.5634	4.3717	4.0350	5.2447

Therefore, it can be predicted that, when the sampling frequency $f_{sa,ac}$ or the modulating-wave frequency f_{ud} is increased, the content of 3rd-order, 5th-order and 7th-order harmonics of i_g is further reduced, which leads to a low value of THD_i. But, the mechanism of their influence is quite different.

As shown in Fig. 19(b), Fig. 20(b) and Table II, when $f_{sa,ac}$ = 10 kHz and f_{ud} = 2 kHz, THD_i = 4.5634%. Compared with Fig. 20(a), in Fig. 20(b), the magnitude of 3rd-order, 5th-order and 7th-order harmonics of the spectrum of i_g is reduced. As indicated above, when $f_{sa,ac}$ is increased, more precise information towards the low-frequency harmonics is acquired in the sampling process, so that the control system can generate the modulating waves with better compensation effect towards those low-frequency harmonics.

As shown in Fig. 19(c), Fig. 20(c) and Table II, when

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$f_{sa,ac} = 2$ kHz and $f_{ud} = 10$ kHz, $\text{THD}_i = 4.3717\%$. There is a quite strange phenomenon. In term of the spectrum of i_g, the magnitude of low-frequency harmonics (such as 3rd-order, 5th-order and 7th-order harmonics) in Fig. 20(c) is larger than those in Fig. 20(b). However, THD_i of Fig. 20(c) is smaller than that of Fig. 20(b). This quite strange phenomenon is consistent with the theoretical analysis about D/A HF-harmonics in the part *B* of Section IV. As f_{ud} is increased, the D/A HF-harmonics contained in v_{ctr}^b or v_{conv} can be shifted to a higher-frequency zone, which leads to a low value of THD_i. Here, the attenuation of $G_h^b(s)$, another effect of increasing f_{ud}, plays a second role to decease THD_i.

As shown in Fig. 19(d), Fig. 20(d) and Table II, when $f_{sa,ac} = 10$ kHz and $f_{ud} = 10$ kHz, $\text{THD}_i = 4.0350\%$. It means that the quality of i_g can be further improved when $f_{sa,ac}$ and f_{ud} are increased at the same time.

Finally, the proposed multirate technique is compared with the original technique, in which $f_{sa,ac}$, f_{ctr} and f_{ud} are set as the same value. The experiment waveforms based on the original technique are shown in Fig. 18(b), where the PETT is under heavy-load condition and $f_{sa,ac} = f_{ctr} = f_{ud} = 5$ kHz. The spectrum of i_g is shown in Fig. 20(e), while the THD values (THD_i) and the magnitude of the fundamental component of i_g is exhibited in Table II. As shown in Table II, when $f_{sa,ac} = f_{ctr} = f_{ud} = 2$ kHz, $\text{THD}_i = 6.5996\%$; and when $f_{sa,ac} = f_{ctr} = f_{ud} = 5$ kHz, $\text{THD}_i = 5.2447\%$. It means that in the original technique, increasing f_{ctr} (also $f_{sa,ac}$ and f_{ud}) is beneficial to decrease THD_i and improve the quality of i_g.

Besides, when $f_{sa,ac} = 10$ kHz, $f_{ctr} = 2$ kHz and $f_{ud} = 2$ kHz, $\text{THD}_i = 4.5634\%$; when $f_{sa,ac} = 2$ kHz, $f_{ctr} = 2$ kHz and $f_{ud} = 10$ kHz, $\text{THD}_i = 4.3717\%$; and when $f_{sa,ac} = 10$ kHz, $f_{ctr} = 2$ kHz and $f_{ud} = 10$ kHz, $\text{THD}_i = 4.0350\%$. In other word, by use of the proposed multirate technique, it can select a relatively low value of f_{ctr} without deteriorating i_g. It is useful in the practical application. For our five-cell PETT laboratory prototype, the computation time of the main control algorithms is $T_{d,ca}^0 > 120\ \mu s$, and the data transmission time is $T_{d,net} > 64$ μs. (For the later one, as 1 MHz optical fibers are adopted and the data with 64 bits need to be transmitted from the main controller to each salve controller, the transmission time is 64×1 μs $= 64$ μs.) Therefore, the effective control period T_{ctr} should be larger than $\left(T_{d,ca}^0 + T_{d,net}\right)$, that is, 184 μs at least. Moreover, with the cell number increased, the fault-diagnosis arithmetic adopted and the control algorithms improved, $\left(T_{d,ca}^0 + T_{d,net}\right)$ may become much larger than 184 μs. Hence, $f_{ctr} = 2$ kHz (or $T_{ctr} = 500$ μs) is selected to increase the time margin of computation and reduce the time occupation of data transmission.

VI. Conclusion

In this paper, two different implementation schemes of carrier-based DPWM are compared at first, including MS-PWM and AS-PWM. Through quantitative analyses, it is proved that there are three problems suffered by AS-PWM, including maximal switching frequency being limited, long modulator delay to make the system unstable and ac input current being distorted. They may restrict the application of AS-PWM in the low-switching-frequency and multi-cell system. On the contrary, these problems don't exist in MS-PWM. Therefore, MS-PWM is recommended in this paper.

On the basis of MS-PWM, and combining with the star-connected distributed structure of the digital control system of PETT, a universal-type multirate structure is proposed, which is suitable for the CHB with low switching frequency and multi cells. By use of the proposed structure, the sampling frequency, control frequency and modulating-wave updating frequency can be separated from the switching frequency, and can be selected as different values respectively according to corresponding practical requirements. This is quite different with the existing technique, where the sampling frequency is set at the same value as the control frequency and AS-PWM is adopted. With the proposed structure,

1) It can better match the distributed hardware and the distributed software to achieve highly efficient utilization of digital chips;

2) It can choose a relatively low control frequency to increase the time margin of computation and reduce the time occupation of data transmission;

3) Relatively high sampling frequency and modulating-wave updating frequency can be selected to improve the steady-state control performance, especially when the control frequency is relatively low.

Appendix

A. Derivation of (4)

As the dominating frequency is v_{ctr}^{d1} is $(1/N)$ of the one of v_{ctr}^d, the relation of them can be represented as

$$v_{ctr}^{d1}[n] = v_{ctr}^d[nN] \tag{14}$$

Define two intermediate sequences $v_{int}^d[n]$ and $\delta_N[n]$, where

$$\delta_N[n] = \begin{cases} 1, & n = 0, \pm N, \pm 2N, \cdots \\ 0, & n = \text{other value} \end{cases} \tag{15}$$

and

$$v_{int}[n] = \delta_N[n] \cdot v_{ctr}^d[n] \tag{16}$$

Making use of the orthogonality property of the basis sequences $e^{j2\pi kn/N}$ $(k = 0,1,\cdots,N-1)$, we can rewrite (15) as

$$\delta_N[n] = \frac{1}{N}\sum_{k=0}^{N-1} e^{-j\frac{2\pi kn}{N}} \tag{17}$$

Denote the z-transform of $v_{int}[n]$, $v_{ctr}^d[n]$ and $v_{ctr}^{d1}[n]$ as $V_{int}(z)$, $V_{ctr}^d(z)$ and $V_{ctr}^{d1}(z)$ respectively. Then, by use of (16) and (17), we arrive at

$$\begin{aligned} V_{int}(z) &= \sum_{n=-\infty}^{\infty} v_{int}[n]z^{-n} = \sum_{n=-\infty}^{\infty} \delta_N[n]v_{ctr}^d[n]z^{-n} \\ &= \frac{1}{N}\sum_{k=0}^{N-1}\left(\sum_{n=-\infty}^{\infty} v_{ctr}^d[n]\left(ze^{j\frac{2\pi k}{N}}\right)^{-n}\right) \\ &= \frac{1}{N}\sum_{k=0}^{N-1} V_{ctr}^d\left(ze^{j\frac{2\pi k}{N}}\right) \end{aligned} \tag{18}$$

Then, based on (14) and (16),

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$$V_{ctr}^{d1}(z) = \sum_{n=-\infty}^{\infty} v_{ctr}^{d1}[n]z^{-n} = \sum_{n=-\infty}^{\infty} v_{int}[nN]z^{-n}$$
$$= \sum_{j=-\infty}^{\infty} v_{int}[j]z^{-\frac{j}{N}} = V_{int}\left(z^{\frac{1}{N}}\right) \quad (19)$$

where $j = nN$. Substitute (18) into (19), we get

$$V_{ctr}^{d1}(z) = \frac{1}{N}\sum_{k=0}^{N-1} V_{ctr}^{d}\left(z^{\frac{1}{N}}e^{-j\frac{2\pi k}{N}}\right)$$

B. Basic Idea to Eliminate the Extra Pulses

As indicated in Section III, if MS-PWM is adopted, extra pulses may generate. In this appendix, the first cell of the CHB is taken as an instance to introduce the generation mechanism of extra pulses and the basic idea to eliminate them. As defined above, i_g is the ac input current and v_{conv1} is the PWM voltage of Cell 1. $v_{conv1} = v_{a_1n_1} - v_{b_1n_1}$. The physical meaning of $v_{a_1n_1}$ and $v_{b_1n_1}$ can be seen in Fig. 3. v_{tri1} is the carrier of Cell 1, and v_{ctr}^b is the *quantized boxcar modulating wave* of Cell 1. The generation mechanism of extra pulses is shown in Fig. 21. As shown in Fig. 21, when extra pulses generate, some power devices will switch on or switch off more frequently. As a result, extra pulses appear in the waveform of the PWM voltage v_{convj}.

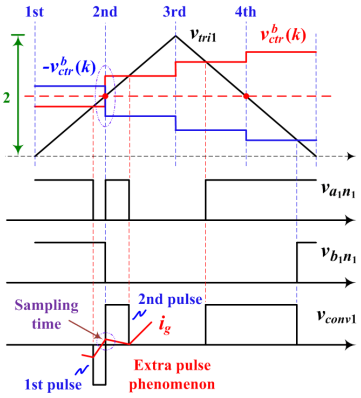

Fig. 21. The generation mechanism of extra pulses.

There are three different methods to completely eliminate the extra pulses. As shown in Fig. 21, the first method is aimed at eliminating the 1st pulse; the second method is aimed at eliminating the 2nd pulse; and the third method is based on the voltage-second conservation principle and aimed at combining the 1st pulse and the 2nd pulse into an equivalent pulse. The former two are easy to be realized, but they may influence the quality of ac input current i_g. There are two reasons:

1) In some operation condition, the pulse width of the 1st pulse and the 2nd pulse is further different, and the variation tendency of i_g will be seriously changed when the pulse with large width is eliminated.

2) As the sampling point of i_g is just at the boundary of these two pulses, serious aliasing may occur at this sampling time and influences the normal operation of the harmonic controllers contained in the inner line current control loop.

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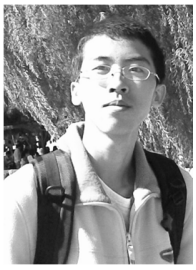

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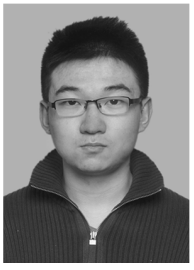

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